CLEAN VERSION OF CLAIMS (AS AMENDED 17 AUGUST 2006)
APPLICATION No. 09/988,940

1. (Currently Amended) Data transmission apparatus for enabling processing of high-rate data streams carrying data cells and delivering the high-rate data streams over a mid-plane having a limited number of signal conductors, the apparatus comprising:

a first demultiplexer for dividing data cells of a high-rate data stream into ***N*** sub-streams, so that each sub-stream carries every N^{th} data cell of the high-rate data stream and data cells in the ***N*** sub-streams are staggered in time with respect to one another;

a plurality of data transmitting devices, each data transmission device associated with a corresponding one of the ***N*** sub-streams for serializing data from the corresponding one of the ***N*** sub-streams and transmitting the serialized data via a corresponding first serial data connection over said mid-plane to a data receive interface;

a first transmit control circuit connected to the data transmitting devices and configured:

to insert flow control signals into one or more of the ***N*** sub-streams, and

to selectively enable and disable the data transmitting devices in response to first receiver enable signals received over said mid-plane from the data receive interface,

whereby cell integrity and sequencing is maintained at said data transmission apparatus, and each of said ***N*** sub-streams has a sub-stream data rate that is ***N*** times lower than a data rate of the high-rate data stream.

2. (Cancelled)

3. (Currently Amended) An apparatus according to claim 1 wherein the data receive interface comprises:

a plurality of data receive devices, each data receive device connected to receive a corresponding sub-stream of data comprising data transmitted by one of the data transmitting devices over the mid-plane via a corresponding one of the first serial connections;

a plurality of buffers, each buffer associated with a corresponding one of the data receive devices and configured to receive fixed-length data cells carried in the corresponding sub-stream; and,

a first receive control circuit configured to determine a sequence of arrival of the fixed-length data cells at the plurality of buffers.

4. (Currently Amended) An apparatus according to claim 3 wherein the first receive control circuit is configured to provide the first receiver enable signals to the first transmit control circuit in response to a status of at least one of the plurality of buffers.

5. (Currently Amended) The apparatus of claim 4 wherein the first receive control circuit is configured to demultiplex the flow control signals from the one or more of the N sub-streams.

6. (Currently Amended) Data transmission apparatus comprising a first transmit interface for transmitting a data stream comprising a sequence of fixed-size transmit cells to a receiver, the first transmit interface comprising:

a first demultiplexer connected to receive the data stream and to split the data stream by delivering the transmit cells in rotation into a plurality of N transmit channels, so that each said transmit channel carries every N^{th} transmit cell;

a plurality of data transmitting devices, each data transmitting device connected to receive the transmit cells of a corresponding one of the N transmit channels and to output the transmit cells of the corresponding one of the N transmit channels on a corresponding data connection for transmitting data over a mid-plane to the receiver, wherein each data transmitting device comprises a serializer device and the corresponding data connection comprises a serial data connection; and,

a first transmit control circuit connected to the data transmitting devices, the first transmit control circuit configured to cause the data transmitting devices to output the transmit cells in sequence with commencement of transmission of the transmit cells from sequential data transmitting devices staggered in time relative to one another by a time difference ΔT;

the apparatus comprising:

a first receive interface comprising:

a plurality of deserializer devices, each of the deserializer devices connected for receiving a corresponding serial stream of receive cells received over the mid-plane from the receiver in a corresponding receive channel;

a plurality of buffers, each of the buffers connected to accept the receive cells from a corresponding one of the deserializer devices and each of the buffers having a capacity sufficient to hold a plurality of the receive cells; and

a first receive control circuit configured to determine a sequence of arrival of the receive cells in the plurality of buffers and to place the receive cells onto a bus in the sequence of arrival;

wherein the first receive control circuit is configured to issue a flow control signal when any one of the buffers has a remaining capacity of Q cells, with $Q \geq 1$ and wherein the first transmit control circuit is configured to transmit the flow control signal with the transmit cells to the receiver.

7. (Currently Amended) The apparatus of claim 6 wherein the first transmit control circuit is configured to multiplex the flow control signal with the transmit cells in one of the transmit channels.

8. (Currently Amended) Data transmission apparatus comprising a first transmit interface for transmitting a data stream comprising a sequence of fixed-size transmit cells to a receiver, the first transmit interface comprising:

a first demultiplexer connected to receive the data stream and to split the data stream by delivering the transmit cells in rotation into a plurality of N transmit channels, so that each said transmit channel carries every N^{th} transmit cell;

a plurality of data transmitting devices, each data transmitting device connected to receive the transmit cells of a corresponding one of the N transmit channels and to output the transmit cells of the corresponding one of the N transmit channels on a corresponding data connection for transmitting data over a mid-plane to the receiver, wherein each data transmitting device comprises a serializer device and the corresponding data connection comprises a serial data connection; and,

a first transmit control circuit connected to the data transmitting devices, the first transmit control circuit configured to cause the data transmitting devices to output the transmit cells in sequence with commencement of transmission of the transmit cells from sequential data transmitting devices staggered in time relative to one another by a time difference ΔT;

wherein:

the first transmit interface is located on a line card having an interface for receiving the data stream,

the receiver is located on a second card, and

the serial data connections comprise data lines extending between the line card and the second card through the midplane.

9. (Currently Amended) The apparatus of claim 8 wherein the receiver comprises a second receive interface, the second receive interface comprising:

a plurality of deserializer devices, each of the deserializer devices connected to a corresponding one of the data connections for receiving the transmit cells of the corresponding one of the N transmit channels after transmission of the transmit cells of the corresponding one of the N transmit channels from the line card to the second card over the mid-plane;

a plurality of buffers, each of the buffers connected to accept the transmit cells from a corresponding one of the deserializer devices and each of the buffers having a capacity sufficient to hold a plurality of the transmit cells; and,

a second receive control circuit configured to determine a sequence of arrival of the transmit cells in the serial data in the plurality of buffers and to place the transmit cells onto a bus in the sequence of arrival.

10. (Currently Amended) The apparatus of claim 9 wherein the second receive control circuit is configured to issue a flow control signal when any one of the buffers has a remaining capacity of Q cells or fewer, with $Q \geq 1$, wherein the second card comprises a transmitter connected to transmit the flow control signal to the line card and wherein the first transmit control circuit is configured, in response to the flow control signal, to inhibit transmission of the transmit cells on at least one of the N transmit channels corresponding to the one of the buffers which has the remaining capacity of Q cells or fewer.

11. (Currently Amended) Data transmission apparatus comprising a first transmit interface for transmitting a data stream comprising a sequence of fixed-size transmit cells to a receiver, the first transmit interface comprising:

a first demultiplexer connected to receive the data stream and to split the data stream by delivering the transmit cells in rotation into a plurality of N transmit channels, so that each said transmit channel carries every N^{th} transmit cell;

a plurality of data transmitting devices, each data transmitting device connected to receive the transmit cells of a corresponding one of the N transmit channels and to output the transmit cells of the corresponding one of the N transmit channels on a corresponding data connection for transmitting data over a mid-plane to the receiver, wherein each data transmitting device comprises a serializer device and the corresponding data connection comprises a serial data connection; and,

a first transmit control circuit connected to the data transmitting devices, the first transmit control circuit configured to cause the data transmitting devices to output the transmit cells in sequence with commencement of transmission of the transmit cells from sequential data transmitting devices staggered in time relative to one another by a time difference ΔT;

wherein:

the first transmit interface is located on a line card having an interface for receiving the data stream,

the receiver is located on a second card, and

the serial data connections comprise data lines extending between the line card and the second card through the midplane;

the receiver comprises a second receive interface, the second receive interface comprising:

a plurality of deserializer devices, each of the deserializer devices connected to a corresponding one of the data connections for receiving the transmit cells of the corresponding one of the N transmit channels after transmission of the transmit cells of the corresponding one of the N transmit channels from the line card to the second card over the mid-plane;

a plurality of buffers, each of the buffers connected to accept the transmit cells from a corresponding one of the deserializer devices and each of the buffers having a capacity sufficient to hold a plurality of the transmit cells; and,

a second receive control circuit configured to determine a sequence of arrival of the transmit cells in the serial data in the plurality of buffers and to place the transmit cells onto a bus in the sequence of arrival;

wherein:

the second receive control circuit is configured to issue a flow control signal when any one of the buffers has a remaining capacity of Q cells or fewer, with $Q \geq 1$;

the second card comprises a transmitter connected to transmit the flow control signal to the line card; and

the first transmit control circuit is configured, in response to the flow control signal, to inhibit transmission of the transmit cells on at least one of the N transmit channels corresponding to the one of the buffers which has

the remaining capacity of Q cells or fewer; and

the transmitter on the second card comprises a second transmit interface for transmitting a second data stream comprising a second sequence of fixed-size second cells to the line card, the second transmit interface comprising:

a second demultiplexer connected to receive the second data stream and to split the second data stream by delivering the second cells in rotation into a second plurality of N second channels so that each said second channel carries every Nth second cell;

a plurality of second serializer devices, each second serializer device connected to receive the second cells of a corresponding one of the N second channels and to output the second cells as serial data on one or more second serial data connections over the mid-plane to the line card; and,

a second transmit control circuit connected to the second serializer devices, the second transmit control circuit configured to cause the second serializer devices to output the second cells of the second data stream in sequence and staggered in time relative to one another by a time difference ΔT.

12. (Previously Presented) Data transmission apparatus comprising:
   a) means for carrying a data stream comprising a sequence of cells having an order;
   b) demultiplexing means for assigning each of the cells of the data stream to one of a plurality of channels;
   c) transmitting means for transmitting the cells in each channel to a receiver by way of signal conductors in a mid-plane;
   d) control means for commencing the transmission of individual cells to the receiver, in the order, at times staggered relative to one another by a time difference ΔT that exceeds a worst case inter-channel difference in latency for transmission of cells from the transmitting means to the receiver by way of the mid-plane; and,
   e) receiving the cells in the order at the receiver.

13. (Cancelled)

14. (Previously Presented) The data transmission apparatus of claim 12 comprising means for receiving a plurality of serially transmitted cells in a plurality of channels and means for determining an order of arrival of the plurality of cells.

15. (Previously Presented) The data transmission apparatus of claim 12 comprising a first receive interface for receiving a data stream, the first receive interface comprising a plurality of receiving devices each for receiving a stream of cells in one of a plurality of channels and, a first receive control circuit configured to determine a sequence of arrival of the cells and to place the cells onto a bus in the sequence of arrival.

16. (Previously Presented) The data transmission apparatus of claim 15 wherein the first receive interface is adapted to receive in the data stream a first direction flow control signal and the first transmit control circuit is connected to receive the flow control signal and adapted to selectively enable or inhibit the transmission of cells by one of the data transmission devices in response to the flow control signal.

17. (Original) The data transmission apparatus of claim 16 wherein the first receive interface is adapted to generate a second direction flow control signal and the first transmit control circuit is adapted to cause one of the data transmitting devices to output the second direction flow control signal.

18. (Currently Amended) A telecommunications switch comprising a plurality of line cards, a switching fabric, a plurality of fabric interface cards connected to the switching fabric and a midplane providing a plurality of data lines connecting the line cards and the fabric interface cards, the telecommunications switch comprising at least one bidirectional interface connecting a line card and a fabric interface card;

the bidirectional interface carrying a first sequence of data cells in a first data stream received at the line card in a first direction from the line card to the fabric interface card and a second sequence of data cells in a second data stream in a second direction from the fabric interface card to the line card;

the bidirectional interface comprising:

a first demultiplexer connected to receive the first data stream and to split the first data stream into a first plurality of N first direction channels so that each first direction channel carries every Nth first direction cell;

for each first direction channel, a first direction serializer device connected to receive the first direction cells of the first direction channel and to output the first direction cells as first direction serial data on one or more first direction serial data connections extending from the line card, through the midplane, to the fabric interface card;

a first transmit control circuit connected to the first direction serializer devices, the first transmit control circuit configured to cause the first direction serializer devices to output the first direction cells in sequence order with commencement of transmission of first direction cells on different first direction channels staggered in time relative to one another by a time difference ΔT;

a plurality of first deserializer devices at the fabric interface card, the first deserializer devices connected to receive and deserialize the first direction serial data on the first direction serial data connections;

a first direction receive control circuit connected to detect an order of arrival of first direction cells on the first direction serial data connections and to place the first direction cells into a first direction received data stream in the order of arrival of the first direction cells;

a second demultiplexer at the fabric interface card and connected to receive the second data stream and to split the second data stream into a second plurality of N second direction channels so that each second direction channel carries every Nth second direction cell;

for each second direction channel, a second direction serializer device

connected to receive the second direction cells of the second direction channel and to output the second direction cells as second direction serial data on one or more second direction serial data connections extending from the fabric interface card, through the midplane, to the line card;

a second transmit control circuit connected to the second direction serializer devices, the second transmit control circuit configured to cause the second direction serializer devices to output the second direction cells in sequence order with commencement of transmission of second direction cells on different second direction channels staggered in time relative to one another by a time difference ΔT;

a plurality of second deserializer devices at the line card, the second deserializer devices connected to receive and deserialize the second direction serial data on the second direction serial data connections; and,

a second direction receive control circuit connected to detect an order of arrival of second direction cells on the second direction serial data connections and to place the second direction cells into a second direction received data stream in the order of arrival of the second direction cells.

19. (Cancelled)

20. (Currently Amended) The method of claim 24 comprising serializing the data on each of the channels before transmitting the data on each of the channels.

21. (Currently Amended) The method of claim 24 wherein there are N channels and assigning the consecutive cells of the data stream into different ones of the plurality of channels comprises assigning the consecutive cells to the channels in rotation so that each channel carries every N^{th} cell.

22. (Currently Amended) The method of claim 20 wherein transmitting the data on each of the channels comprises transmitting a plurality of streams of serial data.

23. (Cancelled)

24. (Currently Amended) A method for transmitting a data stream comprising a sequence of fixed-size cells from a transmitter to a receiver, the method comprising:

assigning consecutive cells of the data stream into different ones of a plurality of channels;

simultaneously transmitting data on each of the channels from the transmitter to the receiver while staggering commencement of transmission of the cells assigned to each channel in time relative to one another by a time difference ΔT;

inhibiting transmission of cells in at least one of the channels in response to receiving, at the transmitter, a first flow control signal issued from the receiver; and,

upon inhibiting transmission of cells in the at least one of the channels:

waiting without transmission of cells in the at least one of the channels; and

after waiting, recommencing transmission of cells in the at least one

of the channels an integer multiple of the time difference ΔT after a time at which transmission of a previous cell commenced on the at least one of the channels.

25. (Currently Amended) The method of claim 20 comprising, for at least one channel, multiplexing a second flow control signal with the data on each of the channels after serializing the data on each of the channels and before transmitting the data on each of the channels.

26. (Currently Amended) The method of claim 20 wherein the sequence of fixed-size cells comprises an OC-192 data stream.

27. (Currently Amended) The method of claim 20 comprising receiving the data on each of the channels at the receiver, deserializing the received data, identifying an order of arrival of received cells at the receiver and placing the received cells on a signal bus in their order of arrival.

28. (Currently Amended) The method of claim 27 comprising, for each channel,
monitoring a number of the received cells which have arrived at the receiver and have not yet been placed on the signal bus; and
suspending transmission of cells on the channel if the number exceeds a threshold.

29. (Currently Amended) The method of claim 28 wherein, for each channel, suspending transmission of cells on the channel comprises issuing a first flow control signal corresponding to the channel and sending the first flow control signal corresponding to the channel from the receiver to the transmitter.

30. (Currently Amended) A method for transmitting a sequence of cells, in order, from a transmitting device to a receiving device, the method comprising:
assigning each of the cells in the sequence to one of a plurality of channels, each of the channels having a recurring cell transmit time, the cell transmit times for successive channels staggered relative to one another by amounts exceeding any inter-channel differences in skew and latency;
in each of the channels, transmitting the cells in the sequence in order of the sequence from the transmitting device to the receiving device over one or more serial data connections and commencing transmission of each cell assigned to the channel only at the cell transmit time for that channel; and,
receiving transmitted cells at the receiving device in the same order that the transmitted cells were transmitted from the transmitting device.

31. (Currently Amended) The method of claim 30 comprising, deserializing the transmitted cells at the receiving device, and detecting an order of arrival of the transmitted cells at the receiving device.

32. (Currently Amended) The method of claim 30 comprising receiving a plurality of cells in the sequence substantially simultaneously at the transmitting device and assigning each of the plurality of cells in the sequence to one of the plurality of channels in rotation.

33. (Currently Amended) An apparatus according to claim 3 comprising means for altering the first receiver enable signals based on a status of at least one of the plurality of buffers.

34. (Currently Amended) An apparatus according to claim 3 comprising means for generating a first receiver enable signal which causes the first transmit control circuit to disable at least one of the data transmitting devices upon arrival, in one of the plurality of buffers, of a second last cell that the one of the plurality of buffers can hold.

35. (Currently Amended) An apparatus according to claim 1 wherein the sub-streams are staggered in time by a period ΔT, and the period ΔT is greater than a maximum total skew due to the mid-plane, the data transmitting device and the data receive interface.

36. (Currently Amended) An apparatus according to claim 1 wherein the flow control signals comprise a clock signal, a parity signal, and a start of cell signal.

37. (New) An apparatus according to claim 1 comprising:

a plurality of data receive devices, each data receive device connected to receive a corresponding sub-stream of data comprising data transmitted from the data receive interface over the mid-plane via a corresponding second serial connection;

a plurality of buffers, each buffer associated with a corresponding one of the data receive devices and configured to receive fixed-length data cells carried in the corresponding sub-stream; and,

a first receive control circuit configured to determine a sequence of arrival of the fixed-length data cells at the plurality of buffers.

38. (New) An apparatus of claim 37 wherein the first receive control circuit is configured to provide the flow control signals to the first transmit control circuit in response to a status of at least one of the plurality of buffers and the flow control signals, when received at the data receive interface over the first serial data connections, cause the data receive interface to inhibit transmission of at least one of the corresponding sub-streams of data over the mid-plane via the corresponding second serial connections.